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IBM Systems & Technology Group

IBM PowerPC 970MP

A new, low-power, high-performance dual-core processor

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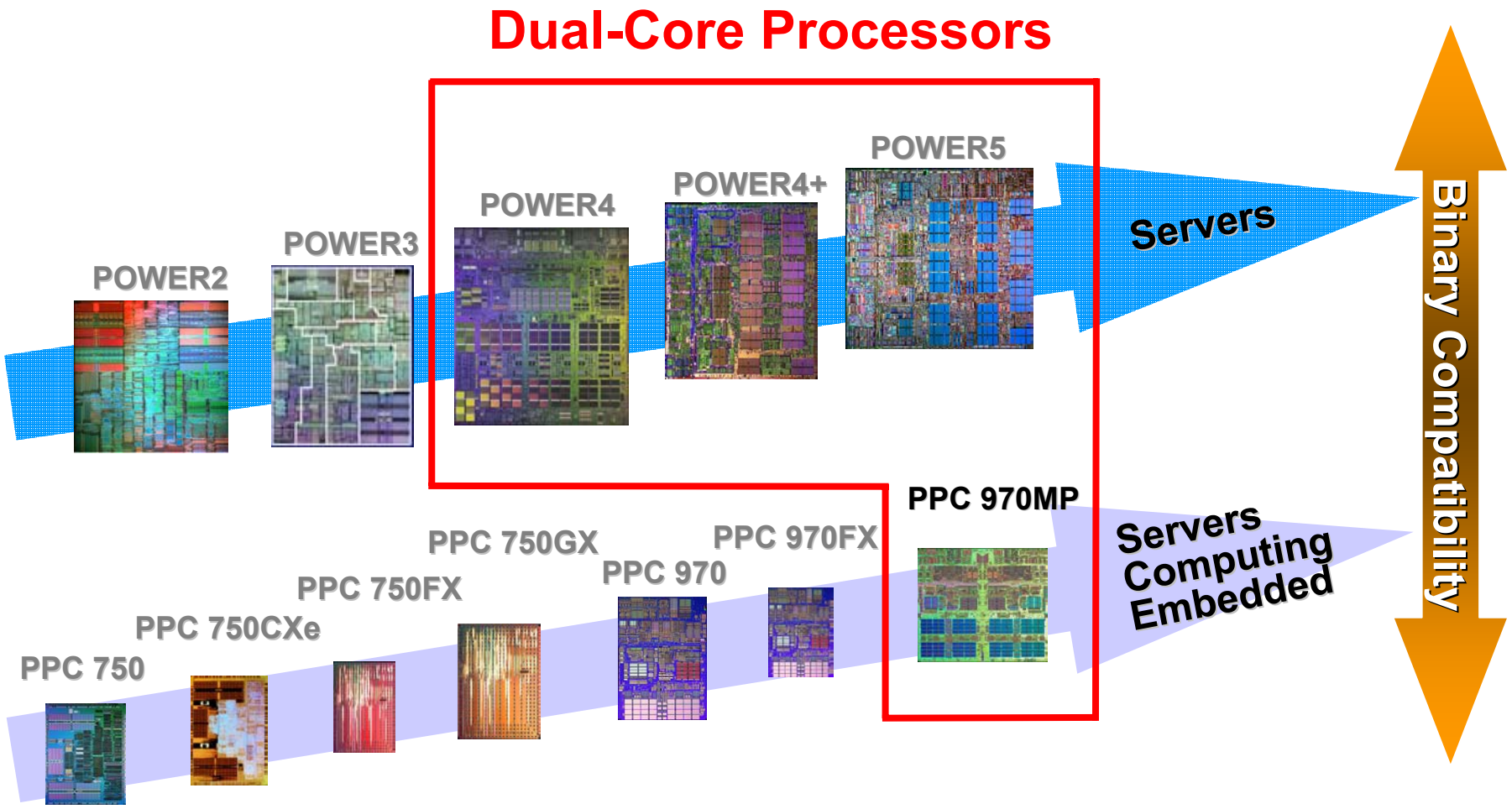
PowerPC 970MP Design Objectives and Overview

- Continue architectural advantages of 64-bit POWER4™ microprocessor for a dual-core PowerPC® processor
- Enhance performance with a larger L2 cache
- Provide wide range of power and performance with frequency tuning, voltage scaling and individual core control
- Continue support of multimedia, graphics and data movement with hardware implementation of a SIMD processing facility
- Continue support of the bandwidth demands of a highly superscalar and SIMD enhanced core through a high speed processor bus

Power Architecture™: The Most Scalable Architecture



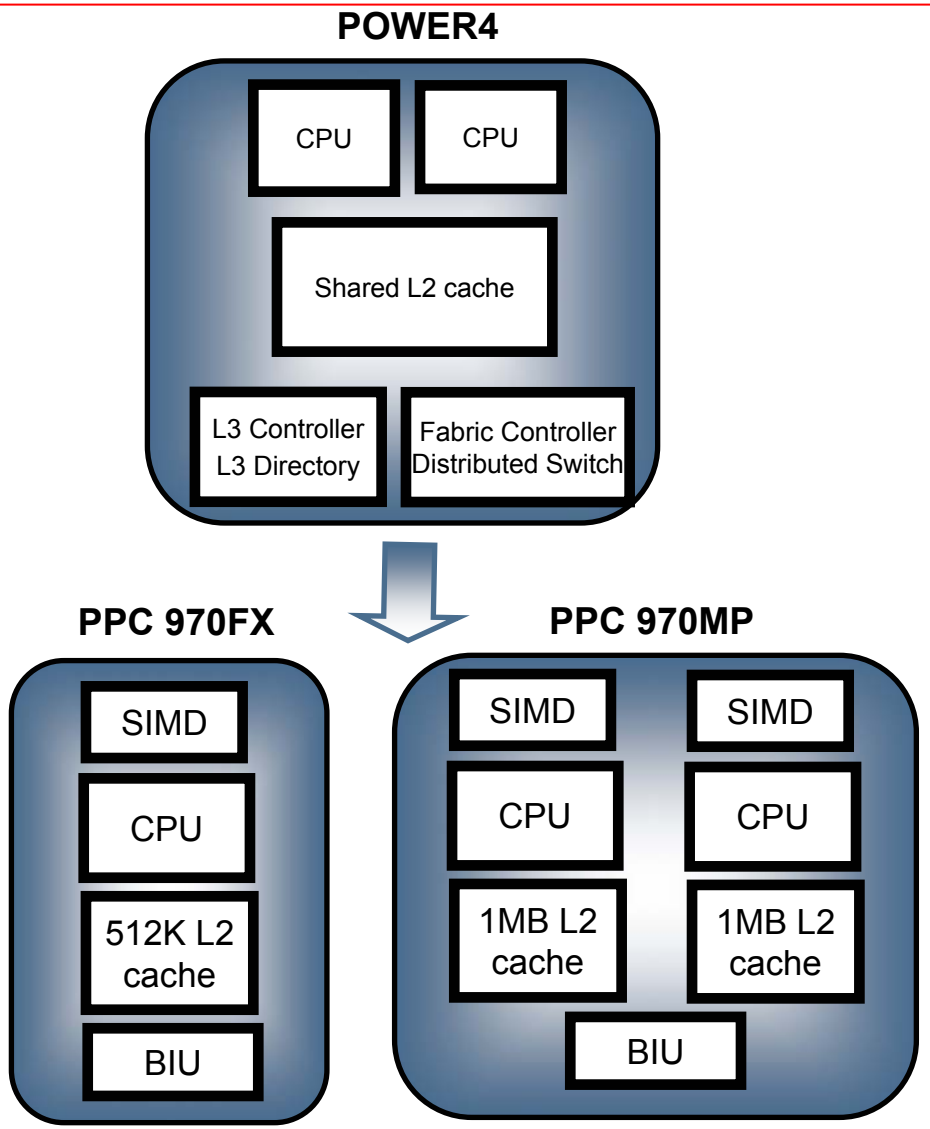
Based on POWER4 Architecture

POWER4 design goals

- Balanced system design
- SMP optimization
- Native 32-bit and 64-bit PowerPC architecture
- High frequency

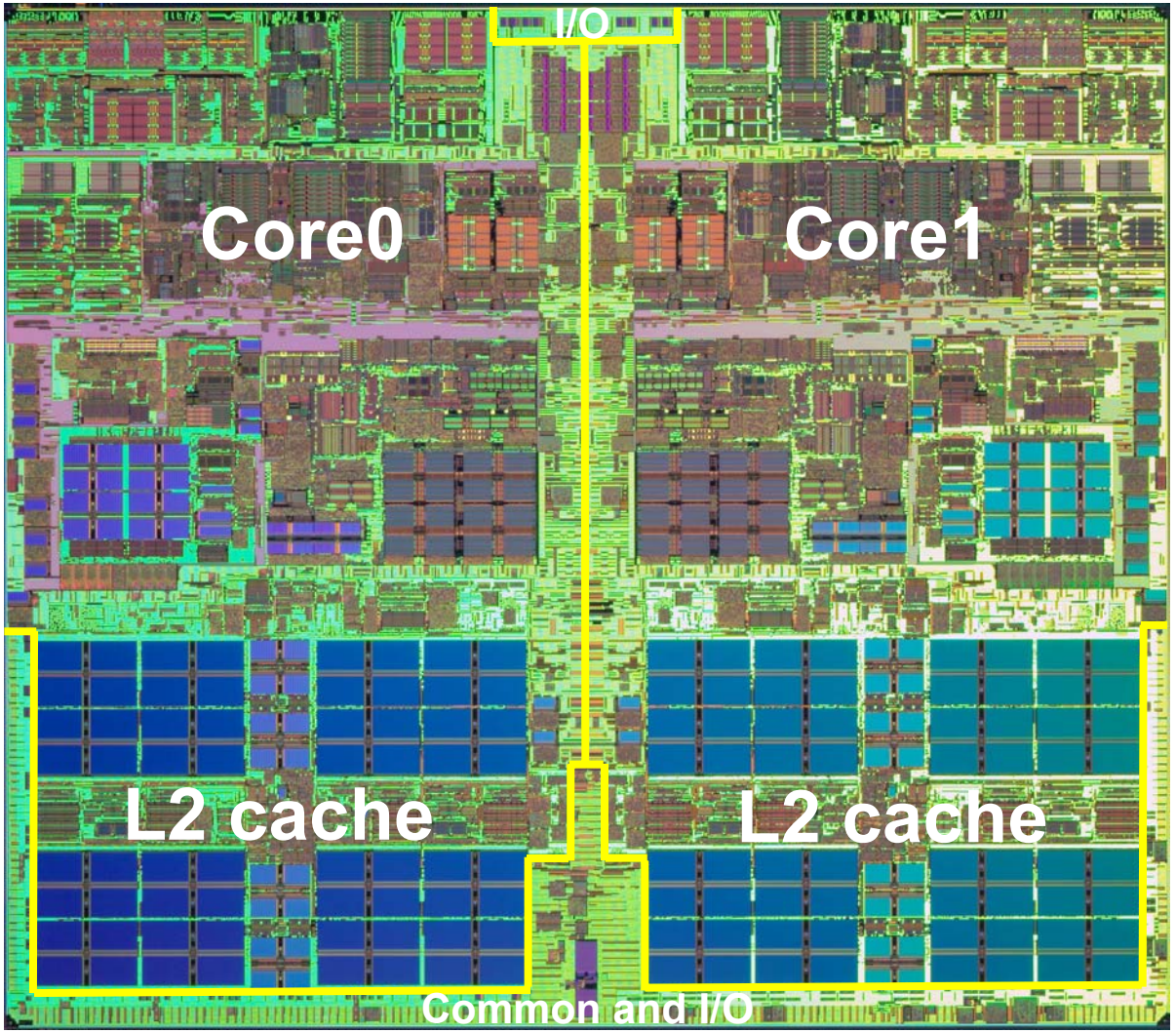
PPC970xx implementations

- Leverage POWER4 architectural advantages
- AltiVec™ SIMD enhanced
- Large L2 caches
- Lower power
- Smaller die
- Enhanced process technology
- Single or dual processor core at higher frequency

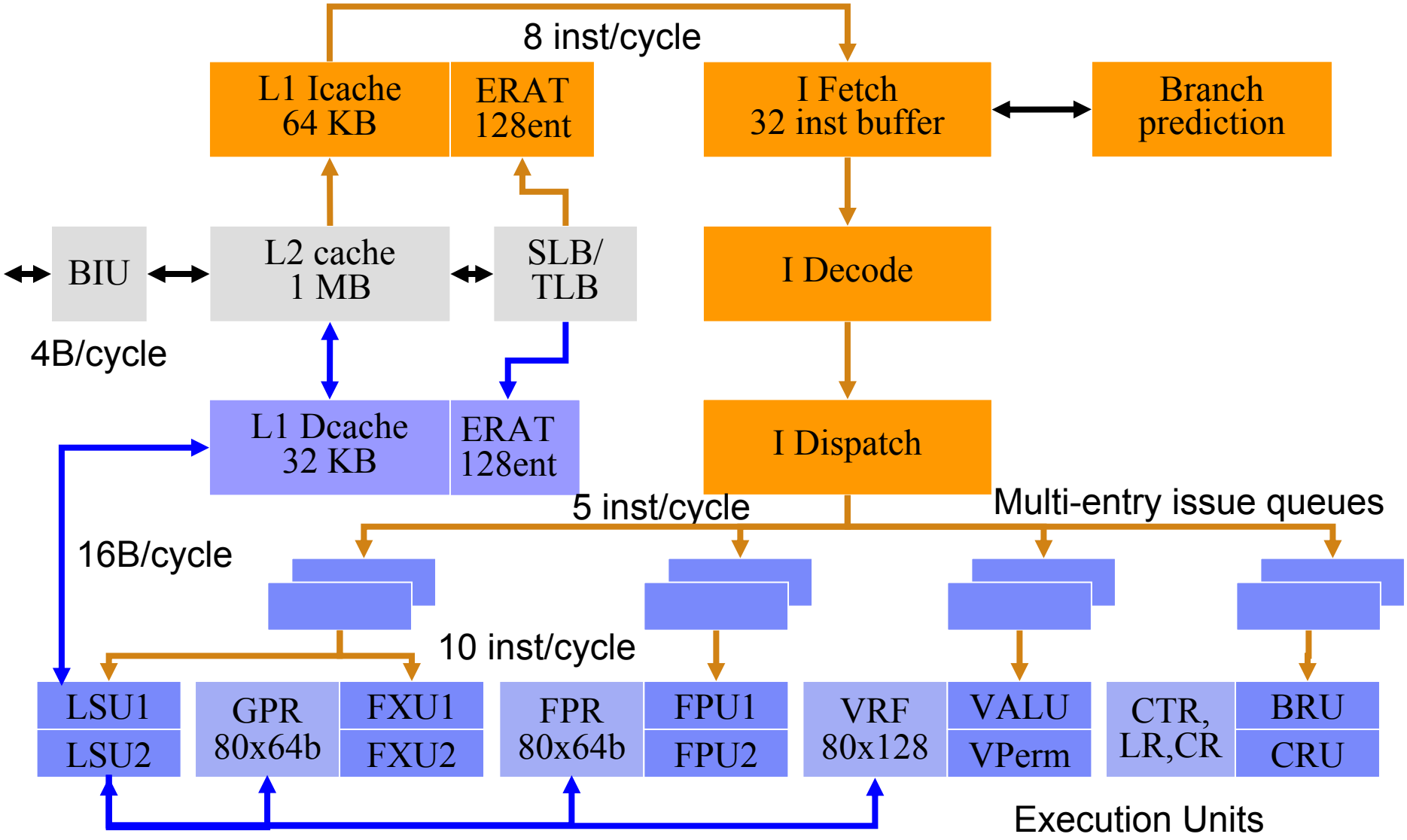


PowerPC 970MP Die Micrograph

- Dual Cores
- Single PLL
- Shared I/O
- Dedicated L2/core

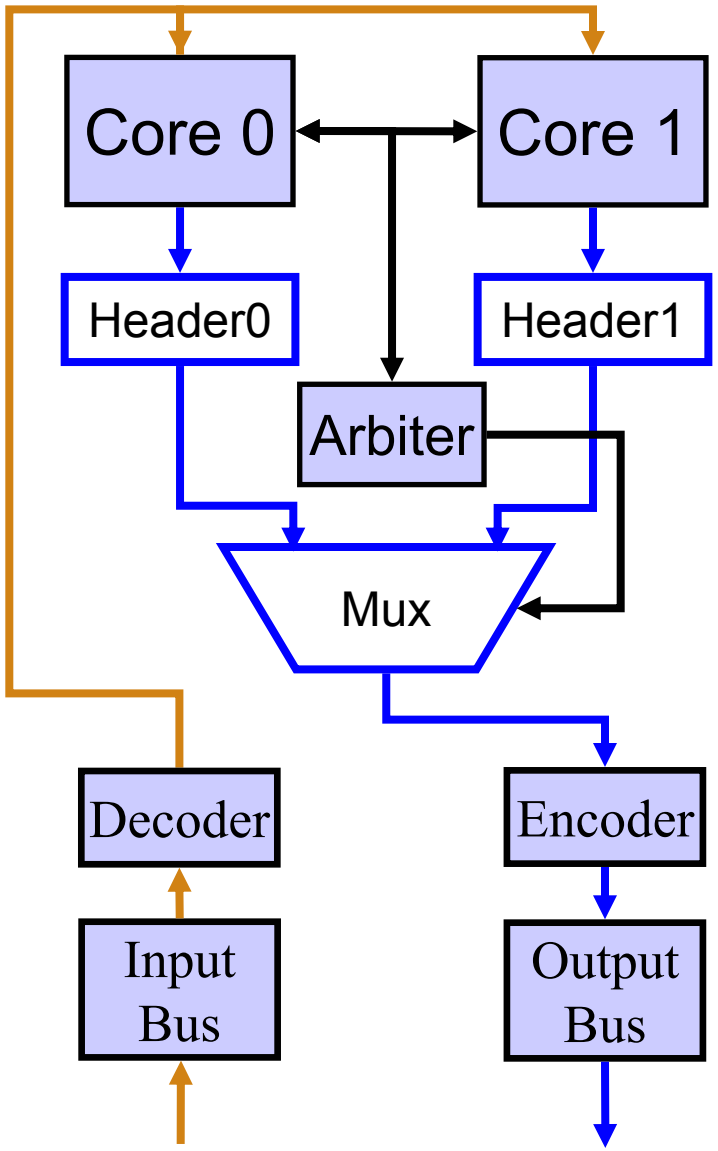


970xx Core Architectural Features



Shared I/O

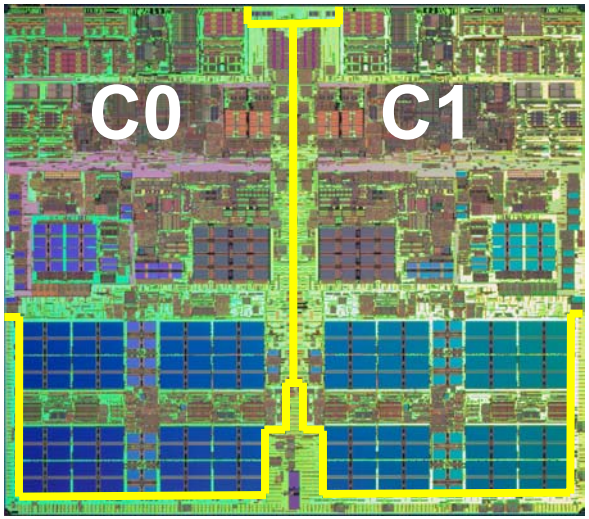
- **Input Bus**
  - Common bus feeds both data and commands to both cores
- **Output Bus**
  - Shared between cores
  - Arbiter controls output mux
  - Round robin technique provides each core with equal access to the output bus
  - Simultaneous requests resolved by granting the bus to the least recent previous requestor



PowerPC 970MP Dual Core Implementation

Individual Core Control

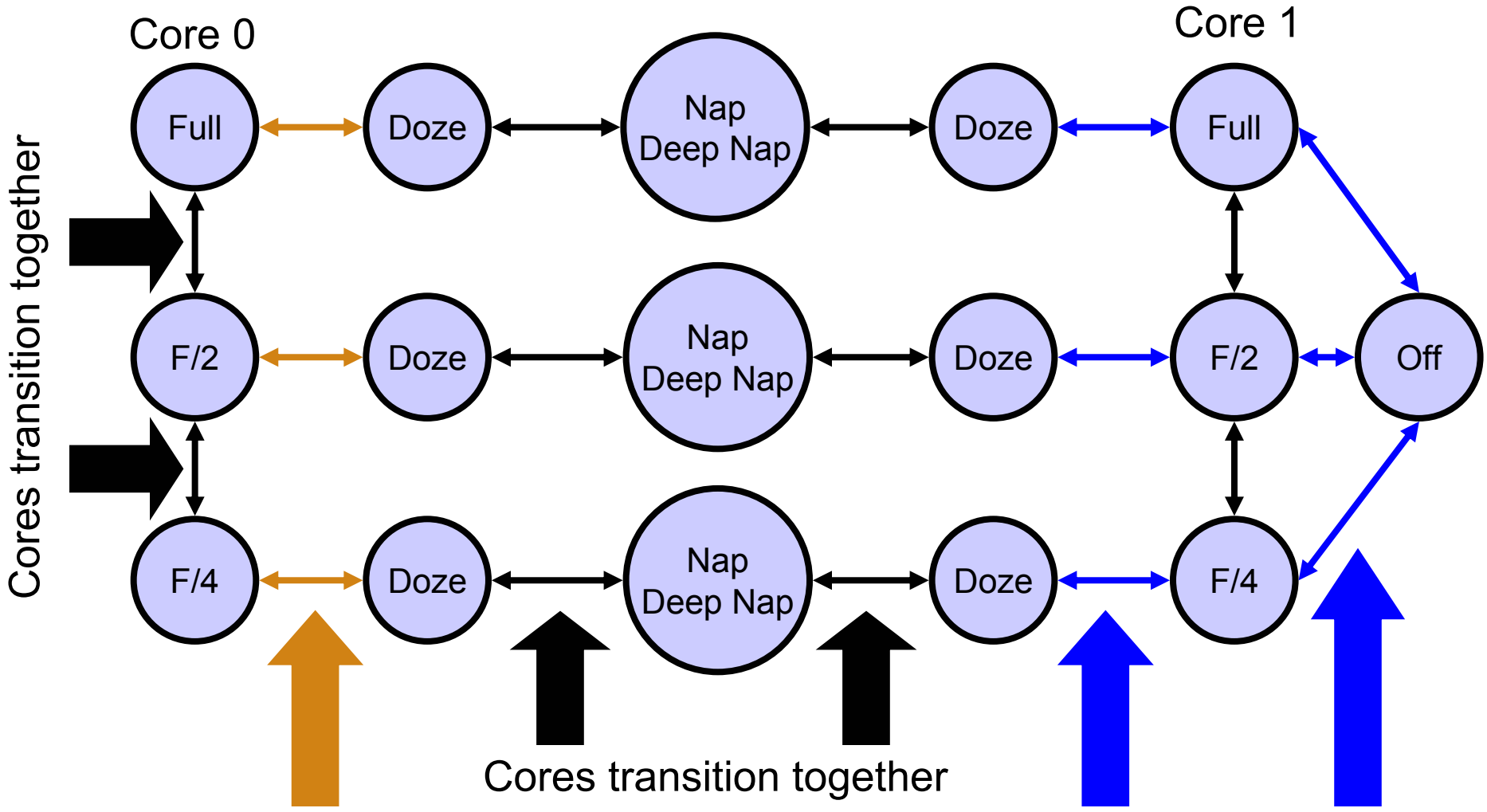
- **Dedicated resets and interrupts**
- **Separate voltage planes on C0 and C1**
  - Independently power down C1
  - Doze mode entered independently
- **Individual Thermal Diode in C0 and C1**
- **Dedicated 1MB L2 cache per core**



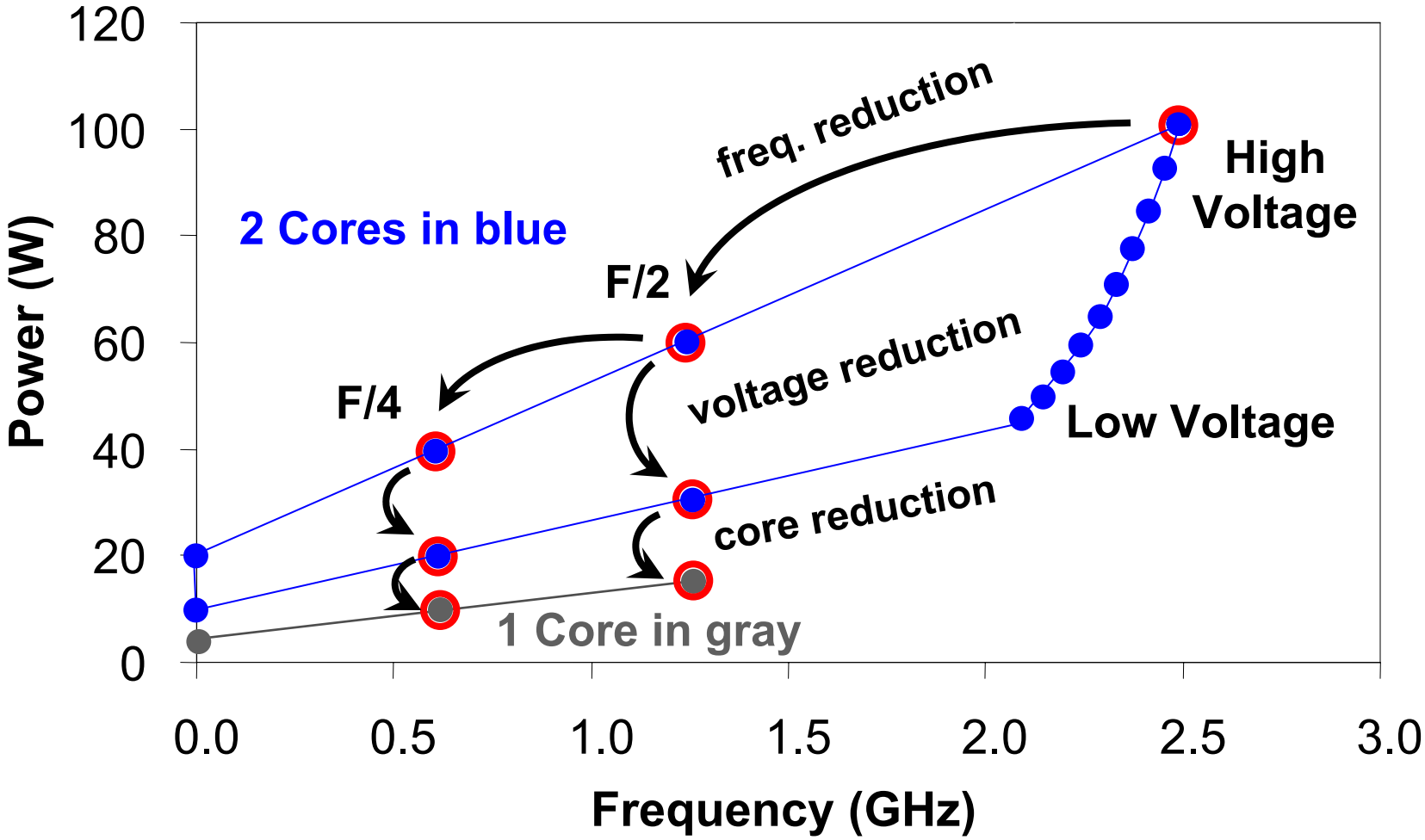
Dual Core Control

- **Frequency control**
  - C0 and C1 run at the same frequency
  - Frequency scaling of the cores is done in unison with the IO bus
- **Power modes**
  - Nap and deep nap modes are entered together
- **Memory coherence maintained through the North Bridge**

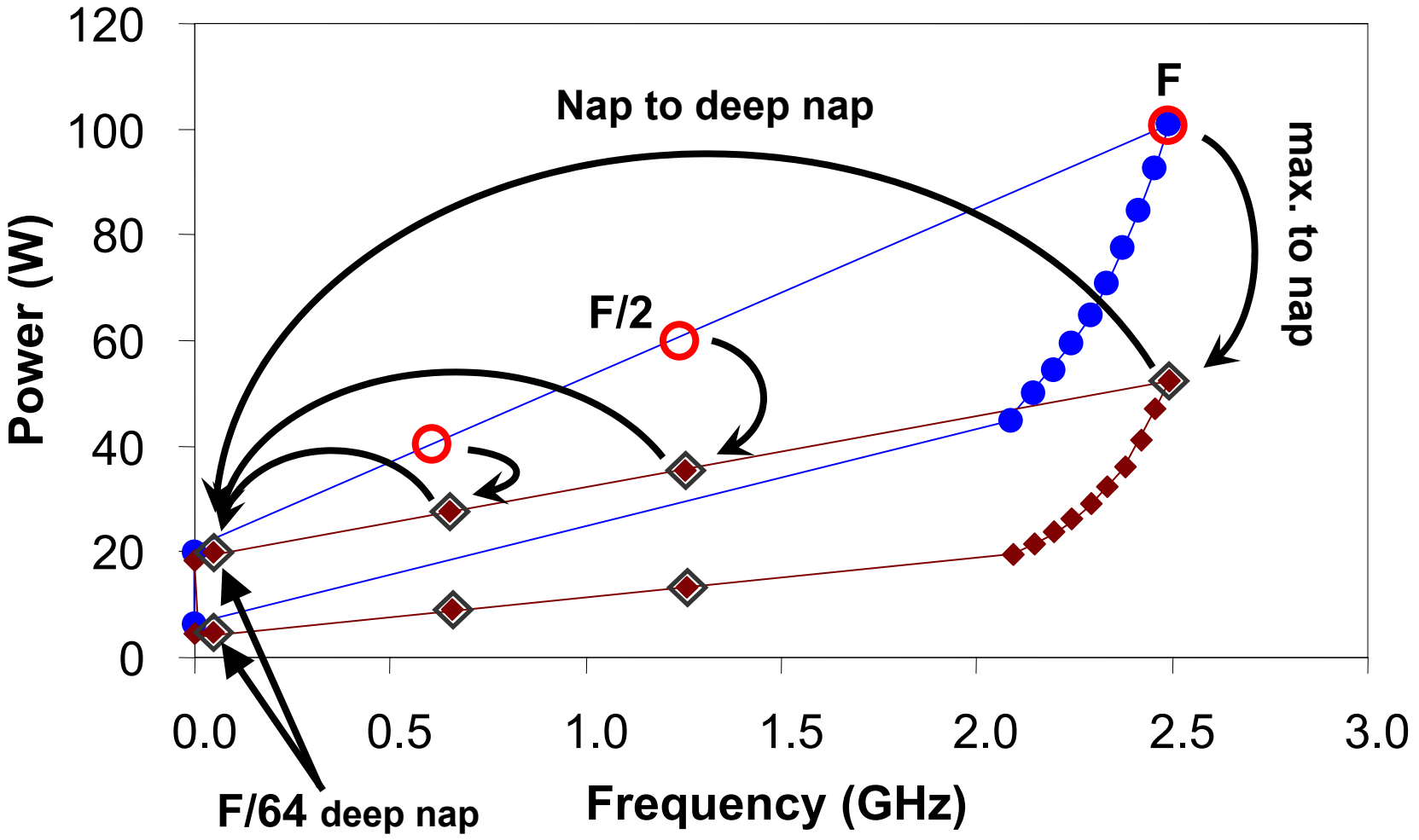
Diagram of Power Modes



Frequency Tuning and Voltage Scaling



Functional to Nap to Deep Nap Transitions



- **Single Core curves not shown**

Typical Power Scaling

		Dual Core		Core 0 only		
Frequency	Power State	High Voltage	Low Voltage	High Voltage	Low Voltage	Relative Perf.
F=2.5GHz	Full	100W		51W		50%
F/2		56W	29W	28W	15W	25%
F/4		36W	18W	18W	9W	12%
F=2.5GHz	Nap	54W		27W		
F/2		35W	16W	18W	9W	
F/4		26W	10W	13W	6W	
F/64	D. Nap	17W	5W	9W	3W	

*Estimation only; subject to change without notice.
Any performance data contained herein is preliminary and subject to change.

PowerPC 970MP Parametrics

Frequencies	1.2 to 2.5GHz+
Architecture	64-bit PowerPC, 32-bit compatible
Performance*	9250 DMIPS/core @ 2.5 GHz 1438 SPECint @ 2.5 GHz (est.) 2076 SPECfp @ 2.5 GHz (est.) 32.3 SPECint_rate @ 2.5 GHz, 2-way (est.) 42.8 SPECfp_rate @ 2.5 GHz, 2-way (est.)
Voltages	1.0-1.35V core logic and 1.3-1.5V I/Os
Typical Dual-Core Power Dissipation*	25W @ 1.2 GHz 100W @ 2.5 GHz
Package	25x25mm CBGA reduced lead 575 pins on 1mm pitch (178 signals)
Technology	90nm, CMOS w/ dual-strained SOI 10 levels of copper interconnect w/low-k dielectric

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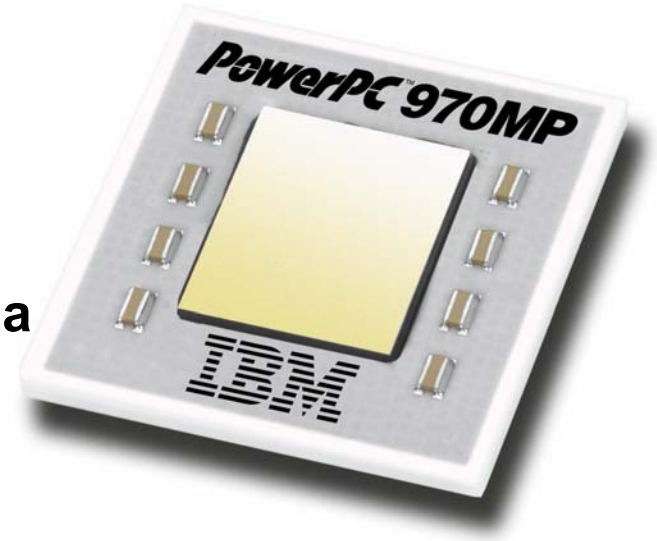
Conclusion

The IBM PowerPC 970MP design constitutes

- Dual 64-bit cores per chip
- Derived from the POWER4 core
- Enhanced with a SIMD/Vector engine
- 1MB L2 cache per core



To achieve high performance on compute and bandwidth intensive applications over a wide power/performance range

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